REMARKS

This Amendment is in response to the Final Office Action mailed April 6, 2004. Applicant has filed a Request for Continued Examination to have the Office withdraw the finality of the Office Action and have this submission entered and considered. In the Office Action, the Examiner rejected claims 1-3, 6-8, 11-13, and 16-18 under 35 U.S.C. § 103. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

Claim 6 has been amended to replace the second instance of "a machine" with --the machine-- to clarify the antecedent basis of the element.

Rejection Under 35 U.S.C. § 102

The Examiner rejects claims 1-3, 6-8, 11-13, and 16-18 under 35 U.S.C. § 103 as being anticipated by Ross et al. (US 5,915,117) in view of the Pentium® Pro Family Developer's Manual, Volume 2: Programmer's Reference Manual.

As per claim 1, the Examiner asserts that Ross discloses a method of handling memory errors, in the form of memory exceptions. Col. 1, lines 13-16.

Applicant has amended claim 1to make clear that the invention is directed to deferring all memory errors, correctable and uncorrectable, as described on page 7 of the specification as filed.

The Examiner states that a General Protection Fault would inherently include faults generated by attempts to access corrupted memory. Applicant respectfully points out that this is incorrect. See Pentium Pro Family Developer's Manual, Volume 3: Operating System Writer's Guide, copyright date 1995, pages 5-37 through 5-38, (OS Guide) submitted herewith. Faults generated by attempts to access corrupted memory may generate a Machine Check Exception. See OS Guide, page 14-1, § 14.1. Applicant is not relying on the distinction between a General Protection Fault and a Machine Check Exception to distinguish over the teaching of Ross. Applicant is merely bringing this to the Examiner's attention to avoid confusion in understanding what was known in the art at the time the application was filed.

Errors generated by attempts to access corrupted memory may be correctable or uncorrectable as described on pages 3-4 of the specification as filed. It is important to note that correctable error do not generate a machine-check exception. See OS Guide, page 14-20, § 14.7.4. As amended, claim 1 is directed to a method of handling memory errors in which all memory errors will provide an error indication that the returned memory value is invalid, and return control of the machine to the executing program if the fault deferral indication is true and the speculative load indication is true. Applicant respectfully submits that this clearly distinguishes the invention as now claimed from the teachings of Ross because a correctable memory error would not generate an exception and Ross teaches that an exception must occur before a deferred exception indicator is written into the destination register. See Ross Fig. 1. Ross does not teach or suggest deferring the correction of a correctable memory error as claimed.

As per claims 2 and 3, applicant relies on the patentability of the claims from which these claims depend to traverse the rejection without prejudice to any further basis for patentability of these claims based on the additional elements recited.

As per claims 6-8, these claims are rejected and traversed on the same basis as discussed above for claims 1-3.

As per claims 11-13, these claims are rejected and traversed on the same basis as discussed above for claims 1-3.

As per claims 16-18, these claims are rejected and traversed on the same basis as discussed above for claims 1-3.

Applicant respectfully requests that the Examiner withdraw the rejection of claims 1-3, 6-8, 11-13, and 16-18 under 35 U.S.C. § 102(b) as being anticipated by Ross.

New Claims

Applicant submits new dependent claims 21-24 that include the elements of the machine further providing first programming model and a second programming model, and providing the error indication that the returned memory value is invalid further requiring that the second programming model be selected as disclosed on page 7 of the specification as filed.

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: December 10, 2004

By _____

James Henry
Reg. No. 41,064
Tel.: (714) 557-3800 (Pacific Coast)